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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/877,640	SMITH
	Examiner	Art Unit
	Thomas L Dickey	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED. (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 September 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *26-192* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *26-192* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) filed 6/8/01 and 9/3/03
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. The preliminary amendments filed on 6/8/2001, 7/27/2001, 10/1/2001, 2/10/2001, and 8/11/2003 have been entered.

Oath/Declaration

2. The oath/declaration filed on 6/8/2001 is acceptable.

Drawings

3. The formal drawings filed on 6/8/2001 are acceptable.

Priority

4. Acknowledgement is made of applicant's claim for domestic priority under 35 U.S.C. 120, through utility patent application number 08/169298 filed December 17, 1993, now US Patent No. 5,545,291.

Information Disclosure Statement

5. The Information Disclosure Statements filed on 6/8/2001 and 9/3/2003 have been considered.

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

A. Claims 47,52,57,70,71,88, and 130-139 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The application, as filed, does not disclose the specific combinations of a laser diode comprising a shaped block of semiconductor material having a length dimension less than or equal to 1 mm in measure, as per claim 130, or an optical detector comprising a shaped block of semiconductor material having a length dimension less than or equal to 1 mm in measure, said block of semiconductor material having a beveled edge adjacent a major surface thereof, as per claim 134. Although there are hints in the specification that some form of the disclosed invention might be useful in the future in building a laser diode or an optical detector, the specifics of the inventions claimed in claims 130-139 are not disclosed. With regard to claim 52, the application as originally filed does not show applicant considered his invention to include a shaped block of material adapted for being received in a recess of a substrate, said shaped block of material having sloped sides and a top surface connected to a bottom surface by said sloped sides, said top surface being substantially parallel to

said bottom surface, said top surface being non-congruent with said bottom surface, wherein said sloped sides have a slope greater than about twenty degrees relative to a line normal to said top surface (although the same device with angles between 40 and 60 degrees is disclosed). With regard to claim 88, the application as originally filed does not show applicant considered his invention to include an electronic chip comprising a block of material separated from a substrate and having a first surface and a second surface substantially parallel to said first surface, said block further having etched side surfaces extending from said first surface to said second surface, said first surface having an areas measurement different than an areal measurement of said second surface, said first surface having a conductive contact disposed thereon, wherein said etched side surfaces have a slope relative to a line normal to said first surface is as little as about twenty degrees (although the same device with angles between 40 and 60 degrees is disclosed). With regard to claim 47, the application as originally filed does not show applicant considered his invention to include an electronic device comprising semiconductor material and having a tapered profile said electronic device having a dimension less than or equal to 1 mm in measure, said electronic device being separated from a substrate, wherein said semiconductor material is a laser diode. With regard to claim 57, the application as originally filed does not show applicant considered his invention to include a shaped block, being an optical detector, of material adapted for being received in a recess of a substrate, said shaped block of material having sloped sides and a top surface connected to a bottom surface by said sloped sides, said top surface being substantially parallel to

said bottom surface, said top surface being non-congruent with said bottom surface. With regard to claims 70 and 71, the application as originally filed does not show applicant considered his invention to include a shaped functional block, being a laser diode or an optical detector, comprising a semiconductor material and having a shape adapted for self-alignment within a shaped recess formed through a substrate surface, said block having a first surface and a second surface and having etched sides which are sloped such that said block fits into said shaped opening only in an orientation where said first surface is exposed through said substrate surface.

B. Claims 37,56,75,83,90,92 and 130-139 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention, to wit: With regard to claim 37 the specification does not teach how to make a structure comprising an assemblage of separate electronic devices, each electronic device comprising a group II-VI compound and having a first surface and a second surface substantially parallel to said first surface, said electronic device further having side surfaces connecting said first surface to said second surface, said first surface having a smaller area than said second surface. Note that to do so requires etching, milling, or otherwise creating a block of group II-VI compound wherein different crystal planes of said group II-VI compound are exposed. With regard to claim 56 the specification does not teach how to make a shaped block of material comprising a group II-VI

compound, adapted for being received in a recess of a substrate, said shaped block of material having sloped sides and a top surface connected to a bottom surface by said sloped sides, said top surface being substantially parallel to said bottom surface, said top surface being non-congruent with said bottom surface. With regard to claim 75 the specification does not teach how to make a semiconductor microstructure comprising a shaped block having a first surface substantially parallel to a second surface, said first surface having an associated first area, said second surface having an associated second area, said first area being larger than said second area, an edge adjacent to said first surface being sloped, said block having a maximum length dimension less than or equal to 1 mm in measure, wherein said shaped block comprises a group II-VI compound. With regard to claim 83 the specification does not teach how to make a portion of an integrated circuit device comprising a shaped functional block having etched sides and comprising a group II-VI compound material and having etched sides and a length dimension less than or equal to 1 mm in measure. With regard to claim 90 the specification does not teach how to make an electronic chip comprising a block of material separated from a substrate and having a first surface and a second surface substantially parallel to said first surface, said block further having etched side surfaces extending from said first surface to said second surface, said first surface having an areas measurement different than an areal measurement of said second surface, said first surface having a conductive contact disposed thereon, wherein said material comprises a multilayered structure including a silicon layer and a gallium arsenide layer. With regard to claim 92 the specifica-

tion does not teach how to make an electronic chip comprising a block of material separated from a substrate and having a first surface and a second surface substantially parallel to said first surface, said block further having etched side surfaces extending from said first surface to said second surface, said first surface having an areal measurement different than an areal measurement of said second surface, said first surface having a conductive contact disposed thereon, wherein said multilayered structure includes a p-type gallium arsenide layer, an n-type gallium arsenide layer, and a eutectic layer, and wherein said multilayered structure further includes a silicon substrate layer, i.e. the multilayered structure includes both a silicon layer and two gallium arsenide layers. With regard to claims 130-139 the specification does not teach how to make a laser diode comprising a shaped block of semiconductor material having a length dimension less than or equal to 1 mm in measure, as per claim 130, or an optical detector comprising a shaped block of semiconductor material having a length dimension less than or equal to 1 mm in measure, said block of semiconductor material having a beveled edge adjacent a major surface thereof, as per claim 134.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 105,179, and 180 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 105,179, and 180 recite the limitation "said amount of semiconductor material" in each of their respective lines 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

A. Claims 26-33,35,36,38,39,43,44, 49-51,53-55, 58-62,64-67,79-82,86,89-91,93, 98-102,142,143,145,151-153,156-158,164-168,171,173-178, and 189 are rejected under 35 U.S.C. 102(b) as being anticipated by TAI (4670770).

(1) With regard to claims 26-33,35,36,38,142, and 143 Tai discloses a structure comprising an assemblage of separate electronic devices (11-12-13-14-15), each electronic device (11-12-13-14-15) having a first (bottom) surface and a second (top) surface substantially parallel to said first surface, said electronic device (11-12-13-14-15) further having side surfaces connecting said first surface to said second surface, said first surface having a smaller area than said second surface, said electronic device (11-12-13-14-15) has a length dimension (5-15 microns, note column 3 line 24) of about 50 microns or less, wherein said electronic device (11-12-13-14-15) has a trapezoidal cross-section, said side surfaces are etched surfaces, said electronic device (11-12-13-14-15) is a multilay-

ered structure, and wherein said multilayered structure includes a metal layer 15 and an insulator (silicon dioxide) layer 14, wherein said electronic device (11-12-13-14-15) comprises material 11 selected from the group consisting of silicon, gallium arsenide, aluminum gallium arsenide, diamond, and germanium, specifically, GaAs, which is a group III-V compound, wherein the perimeter of said first surface has a rectangular shape, wherein said electronic device (11-12-13-14-15) has an edge portion that is beveled, and said electronic device (11-12-13-14-15) is shaped like a truncated pyramid. Note figures 1,3,4, column 2 lines 45-49, and column 3 lines 20 and 24 of Tai.

(2) With regard to claims 39,43,44, and 145 Tai discloses an electronic device (11-12-13-14-15) comprising semiconductor material 11 and having a tapered profile, said electronic device (11-12-13-14-15) having a dimension (5-15 microns, note column 3 line 24) less than or equal to 1 mm in measure and in fact being less than 50 microns, said electronic device (11-12-13-14-15) being separated from a substrate 21, wherein said semiconductor material is a group III-V compound, specifically, gallium arsenide. Note figures 1,3,4, column 2 lines 45-49, and column 3 lines 20 and 24 of Tai.

(3) With regard to claims 49-51,53,54,55,58 and 151-153 Tai discloses a shaped block (11-12-13-14-15) of multilayered material having a length dimension (5-15 microns, note column 3 line 24) of about 50 microns or less, adapted for being received in a recess of a substrate 21, said shaped block (11-12-13-14-15) of material having sloped sides and a top surface connected to a bottom surface by said sloped sides, said top surface being substantially parallel to said bottom surface, said top surface being non-congruent

with said bottom surface, wherein said sloped sides are etched, said material comprises a multilayered structure, including gallium arsenide, a group III-V compound, wherein the perimeter of said top surface has a rectangular shape, wherein said sloped sides have a trapezoidal profile and define a portion of a beveled edge, and wherein said shaped block has a shape of a truncated pyramid. Note figures 1,3,4, column 2 lines 45-49, and column 3 lines 20 and 24 of Tai.

(4) With regard to claims 59-62,64-67, and 156-158, Tai discloses a shaped functional block (11-12-13-14-15) comprising a semiconductor material 11 and having a shape adapted for self-alignment within a shaped recess formed through a substrate 21 surface, said block (11-12-13-14-15) having a first surface and a second surface and having etched sides which are sloped such that said block (11-12-13-14-15) fits into said shaped opening; only in an orientation where said first surface is exposed through said substrate 21 surface, wherein said first surface includes a conductive contact 13 disposed thereon and said first surface has an area smaller than said second surface, said first surface has a circular perimeter, a rectilinear perimeter, or an octagonal perimeter, further comprising a multilayered structure wherein said multilayered structure includes a metal layer 15 and a silicon dioxide insulator layer 14, wherein said etched sides are characterized by having a trapezoidal profile, said etched sides form a beveled edge adjacent said first surface, and the functional block (11-12-13-14-15) has the shape of a truncated pyramid. Note figures 1,3,4, column 2 lines 45-49, and column 3 lines 20 and 24 of Tai.

(5) With regard to claims 79-82 and 164-168, Tai discloses a portion of an integrated circuit device comprising a shaped functional block (11-12-13-14-15), said functional block (11-12-13-14-15) comprising a semiconductor material and having a length dimension less than or equal to 1 mm in measure, and less than or equal to 500 microns, and in fact less than or equal to 50 microns in measure, said functional block (11-12-13-14-15) having etched sides, wherein said semiconductor material is a multilayered structure selected from the group consisting of silicon, gallium arsenide, aluminum gallium arsenide, diamond, and germanium, specifically, gallium arsenide, a group III-V compound, and wherein said etched sides have the form of a trapezoidal profile, said functional block (11-12-13-14-15) further comprises a first major surface and a second major surface connected to said first major surface by said etched sides, a portion of said etched sides adjacent to said first major surface forming a beveled edge, and said functional block (11-12-13-14-15) has a shape of a truncated pyramid. Note figures 1,3,4, column 2 lines 45-49, and column 3 lines 20 and 24 of Tai.

(6) With regard to claims 86,89-91,93,98,171, and 173-175, Tai discloses an electronic chip comprising a block of material (11-12-13-14-15) separated from a substrate 21 and having a first surface and a second surface substantially parallel to said first surface, said block further having etched side surfaces extending from said first surface to said second surface, said first surface having an areal measurement different than an areal measurement of said second surface, said first surface having a conductive contact disposed thereon, wherein said material comprises a multilayered structure including one or

more layers of semiconductor material, said multilayered structure includes a p-type gallium arsenide layer, an n-type gallium arsenide layer, and a eutectic layer, said material is semiconductor material, a cross-section thereof shows one of a cylindrical shape, a rectangular shape, a square shape, a hexagonal shape, a T-shape, and a kidney shape, and wherein said shaped block has an outwardly sloped profile, a profile of said shaped block resembles a trapezoid, said etched side surfaces define a beveled edge adjacent said first surface, and said shaped block is one of a pyramid shape and a truncated pyramid shape. Note figures 1,3,4, column 2 lines 45-49, and column 3 lines 20 and 24 of Tai.

(7) With regard to claims 99-102 and 176-178, Tai discloses an electronic chip comprising a shaped functional block (11-12-13-14-15)including a semiconductor material 11, said functional block having tapered sides with a top surface and a bottom surface smaller than said top surface, a conductive contact 13 or 15 disposed atop either or both said top surface and said bottom surface, said functional block further having a length dimension less than or equal to 1 mm in measure, less than or equal to 500 microns, and in fact less than or equal to 50 microns, a perimeter of said top surface having a rectilinear shape, a circular shape, or an octagonal shape, wherein said top surface is substantially parallel to said bottom surface, said semiconductor material is a multilayered structure, and said tapered sides define at least a beveled edge adjacent said top surface. Note figures 1,3,4, column 2 lines 45-49, and column 3 lines 20 and 24 of Tai.

(8) With regard to claim 189 Tai discloses a shaped block (11-12-13-14-15)of semiconductor material having tapered sides, said block of material comprising a first surface

and a second surface in substantially parallel relation to said first surface, said tapered sides defining a beveled edge adjacent at least one of said first and second surfaces. Note figures 1,3,4, column 2 lines 45-49, and column 3 lines 20 and 24 of Tai.

B. Claims 26,30,34, 39,40-42,48, 49, 86,104,106-109, 123-129, 140,141,144, 146-150,172, and 186-188 are rejected under 35 U.S.C. 102(b) as being anticipated by NG et al. (H208).

(1) With regard to claims 26,30,34,140, and 141, Ng et al. discloses a structure comprising an assemblage of separate electronic devices 14, each electronic device 14 being a multilayered structure including a layer of silicon nitride and having a length measurement (the depth of the block being .25-.75 mm) less than or equal to 1 mm, and in fact less than or equal to 500 microns, and a first (top) surface and a second (bottom) surface substantially parallel to said first surface, said electronic device 14 further having side surfaces connecting said first surface to said second surface, said first surface having a smaller area than said second surface. Note figures 4-7 and column 3 lines 2-3 and column 4 lines 12-19 and 33-35 of Ng et al.

(2) With regard to claims 39,40,41,42,48,144,146,147, and 148, Ng et al. discloses an electronic device 14 comprising multilayered semiconductor material and having a tapered profile, said electronic device 14 having a dimension (the depth of the block being .25-.75 mm) less than or equal to 1 mm in measure and in fact less than or equal to 500 microns, said electronic device 14 being separated from a substrate 10, further having a first (top) surface and a second (bottom) surface substantially parallel to said first surface,

wherein the perimeter of said first surface has a rectangular shape, an octagonal shape, or a circular shape, a cross-section thereof shows one of a cylindrical shape, a rectangular shape, a square shape, a hexagonal shape, a T-shape, and a kidney shape, said profile has a trapezoidal shape and at least a partially beveled edge, and wherein the electronic device 14 has one of a pyramid shape and a truncated pyramid shape. Note figures 4-7 and column 3 lines 2-3 and column 4 lines 12-19 and 33-35 of Ng et al.

(3) With regard to claims 49,149, and 150, Ng et al. discloses a shaped block of material 14 having a length measurement (the depth of the block being .25-.75 mm) less than or equal to 1 mm, and in fact less than or equal to 500 microns, said shaped block of material 14 having sloped sides and a top surface connected to a bottom surface by said sloped sides, said top surface being substantially parallel to said bottom surface, said top surface being non-congruent with said bottom surface. Note figures 4-7 and column 3 lines 2-3 and column 4 lines 12-19 and 33-35 of Ng et al.

(4) With regard to claims 86 and 172, Ng et al. discloses a electronic chip comprising a block of material 14 separated from a substrate 21 and having a first surface and a second surface substantially parallel to said first surface, said block further having etched side surfaces extending from said first surface to said second surface, said first surface having an areal measurement different than an areal measurement of said second surface, said first surface having a conductive contact disposed thereon, wherein said shaped block has an inwardly sloped profile. Note figures 3 and 4, columns 3 lines 3-6 and 23-34 and column 4 lines 1-5 of Ng et al.

(5) With regard to claims 104 and 106-109, Ng et al. discloses a electronic component 14 separated from a first substrate 21 comprising a first (top) surface; a conductive contact 18 disposed atop said first surface; a second surface in substantially parallel relation to said first surface; and etched (side) surfaces connecting said first surface to said second surface, said etched surfaces being tapered to define at least a beveled edge to said first surface, wherein said electronic component 14 is adapted for self-alignment within a shaped opening through a surface of a second substrate, should such a second substrate present itself. With regard to claims 123-129 and 186-188, Ng et al. discloses a device comprising a block 14 of semiconductor material, said block 14 having a top surface, the perimeter of said top surface having a rectangular shape, and a bottom surface connected to said top surface by etched sloped surfaces defining a beveled edge adjacent one of said top and bottom surfaces, said block 14 having a length dimension less than or equal to 1 mm in measure and in fact less than or equal to 500 microns. Note figures 3 and 4, columns 3 lines 3-6 and 23-34 and column 4 lines 1-5 of Ng et al.

The applicant's claims 106-109 and 125-128 do not distinguish over the Ng et al. reference regardless of the process used to form said etched surfaces, because only the final product is relevant, not the recited processes of wet etching, mask edging, reactive ion etching, or ion milling. It is noted that these processes are exclusive alternates, only one may be used. Since applicant claims that any of them may make the claimed invention, it is impossible for any single one of them to leave a distinguishing mark on the

claimed invention, unless somehow all of them leave that mark. As noted below, case law assigns applicant the burden of showing how such a mark is left.

Note that a "product by process" claim is directed to the product per se, no matter how actually made. In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above caselaw makes clear. See also MPEP 706.03(e).

Note further that in claims 123-128 and 186-188, the recitations "A light-emitting diode (LED)" and "The LED of" have not been given patentable weight because the recitations occur in the preambles. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See In re Hirao, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and Kropa v. Robie, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

A. Claims 45,46,94-97, and 110 are rejected under 35 U.S.C. 103(a) as being unpatentable over NG et al. (H208) in view of FANG et al. (IBM Technical Disclosure, vol. 19, No. 10, Mar. 1977, pp. 3959-3960).

(1) Ng et al. discloses an electronic device comprising semiconductor material and separated from a substrate, having all the limitations of claims 45 and 46 except that said semiconductor material is a light-emitting diode, specifically a gallium arsenide light-emitting diode. Note figures 3 and 4, columns 3 lines 3-6 and 23-34 and column 4 lines 1-5 of Ng et al. However, Fang et al. discloses an electronic device comprising semiconductor material 2-3-4-7-8 and separated from a substrate 10, with a light-emitting diode, specifically a gallium arsenide light-emitting diode. Note figure 2 of Fang et al. Therefore, it would have been obvious to a person having skill in the art to augment Ng et al.'s electronic device comprising semiconductor material and separated from a substrate with the light-emitting diode, specifically the gallium arsenide light-emitting diode such as taught by Fang et al. in order to provide a device having silicon active circuits for logic

and power, along with high energy band gap II-V active circuits for optoelectronics, to thus merge semiconductor optoelectronics with silicon technology.

(2) Ng et al. discloses an electronic chip comprising a block of material separated from a substrate, having all the limitations of claims 94-97 except that said electronic chip is a light-emitting diode or a gallium arsenide diode, specifically a gallium arsenide microwave device, more specifically a gallium arsenide resonant tunneling diode. Note figures 3 and 4, columns 3 lines 3-6 and 23-34 and column 4 lines 1-5 of Ng et al. However, Fang et al. discloses an electronic chip comprising a block of material 2-3-4-7-8 separated from a substrate 10, with a light-emitting diode or a gallium arsenide diode, specifically a gallium arsenide microwave device, more specifically a gallium arsenide resonant tunneling diode. Note figure 2 of Fang et al. Therefore, it would have been obvious to a person having skill in the art to augment Ng et al.'s electronic chip comprising a block of material separated from a substrate with the light-emitting diode or a gallium arsenide diode, specifically a gallium arsenide microwave device, more specifically a gallium arsenide resonant tunneling diode such as taught by Fang et al. in order to provide a device having silicon active circuits for logic and power, along with high energy band gap II-V active circuits for optoelectronics, to thus merge semiconductor optoelectronics with silicon technology.

(3) Ng et al. discloses an electronic component separated from a first substrate, having all the limitations of claim 110 except that the electronic component is a light-emitting diode. Note figures 3 and 4, columns 3 lines 3-6 and 23-34 and column 4 lines 1-5 of Ng

et al. However, Fang et al. discloses an electronic component 2-3-4-7-8 separated from a first substrate 10, with a light-emitting diode. Note figure 2 of Fang et al. Therefore, it would have been obvious to a person having skill in the art to augment Ng et al.'s electronic component separated from a first substrate with the light-emitting diode such as taught by Fang et al. in order to provide a device having silicon active circuits for logic and power, along with high energy band gap II-V active circuits for optoelectronics, to thus merge semiconductor optoelectronics with silicon technology.

B. Claims 63, 87,154,155,169,170, and 190-192 are rejected under 35 U.S.C. 103(a) as being unpatentable over TAI (4670770) in view of GARDNER et al. (5055892).

With regard to claims 63,154, and 155, Tai discloses a shaped functional block having all the limitations of claims 63,154, and 155 except that said functional block has a maximum length dimension less than or equal to 1 mm in measure (500 microns or less, per claim 170, 50 microns or less, per claim 87). Note the explanation regarding claim 59 in section 7A above. Further, with regard to claims169, 170, and 87, Tai discloses an electronic chip comprising a block of material having all the limitations of claims 169,170, and 87 except that said block of material has a width of about 1 mm or less (500 microns or less, per claim 170, 50 microns or less, per claim 87) and a length of about 1 mm or less (500 microns or less, per claim 170, 50 microns or less, per claim 87). Note the explanation regarding claim 86 in section 7A above. Further, with regard to claims 190,191, and 192, Tai discloses a shaped block of semiconductor material having all the limitations of claims 190,191, and 192 except that the shaped block has a maximum length dimension

less than or equal to 1 mm in measure (500 microns in measure, per claim 191, 50 microns in measure, per claim 192). Note the explanation regarding claim 189 in section 7A above. Tai does not disclose the 50 micron to 1 mm scale for the shaped functional block (aka "shaped block" or simply "block of material") as claimed by the applicant, in fact Tai makes no mention whatsoever of any kind of scale for the shaped functional block. Given that Tai's device is in fact fully disclosed, this lack of mention indicates that it may have been within the skill of one having skill in the art to determine the proper scale for himself.

Gardner et al. discloses a device with a shaped functional block, being in Gardner et al.'s version a functioning LED, having typical dimensions of 250 microns length, breadth, and depth. Note column 6 lines 25-26 Gardner et al. Therefore, it would have been obvious to a person having skill in the art to scale Tai's shaped functional block in the ranges 50 microns to 1 mm, such as taught by Gardner et al. in order to build the shaped functional block (aka "shaped block" or simply "block of material") in the scale ranges typically known to the art at the time of the invention. Although neither Gardner et al. nor Tai disclose the 50 micron scale for the shaped functional block it has recently been observed that a *prima facie* case of obviousness typically exists when the ranges of a component of the claimed invention overlap the ranges disclosed in the prior art or when the ranges of the component do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. *In re Peterson*, 65 USPQ2d 1379 (CA FC 2003). It appears that in this case, one skilled in the art would have expected a 50 micron shaped functional block (aka "shaped block" or simply "block of mate-

rial") to have the same properties as the 250 micron shaped functional block disclosed by Gardner et al.

C. Claim 68 is rejected under 35 U.S.C. 103(a) as being unpatentable over TAI (4670770) in view of NG et al. (H208).

Tai discloses a shaped functional block all the limitations of claim 68 except a silicon nitride layer in the multilayered structure of the shaped functional block. Note figures 1,3,4, column 2 lines 45-49, and column 3 lines 20 and 24 of Tai.

However, Ng et al. discloses shaped functional block with a silicon nitride layer in a multilayered structure. Note column 4 lines 15-17 of Ng et al. Therefore, it would have been obvious to a person having skill in the art to add a silicon nitride layer to Tai's shaped functional block such as taught by Ng et al. in order to provide an etch stop layer.

D. Claims 69,84,85,94-97, and 103 are rejected under 35 U.S.C. 103(a) as being unpatentable over TAI (4670770) in view of FANG et al. (IBM Technical Disclosure, vol. 19, No. 10, Mar. 1977, pp. 3959-3960).

(1) Tai discloses a shaped functional block comprising a semiconductor material and having a shape adapted for self-alignment within a shaped recess formed through a substrate surface, having all the limitations of claim 69 except that the functional block is a light-emitting diode. Note figures 1,3,4, column 2 lines 45-49, and column 3 lines 20 and 24 of Tai. However, Fang et al. discloses a semiconductor material 2-3-4-7-8 within a shaped recess formed through a substrate surface 10 with a light-emitting diode. Note figure 2 of Fang et al. Therefore, it would have been obvious to a person having skill in

the art to augment Tai's shaped functional block comprising a semiconductor material and having a shape adapted for self-alignment within a shaped recess formed through a substrate surface with the light-emitting diode such as taught by Fang et al. in order to provide a device having silicon active circuits for logic and power, along with high energy band gap II-V active circuits for optoelectronics, to thus merge semiconductor optoelectronics with silicon technology.

(2) Tai discloses a portion of an integrated circuit device comprising a shaped functional block, said functional block comprising a semiconductor material, having all the limitations of claims 84 and 85 except that said semiconductor material constitutes a light-emitting diode, specifically a gallium arsenide light-emitting diode. Note figures 1,3,4, column 2 lines 45-49, and column 3 lines 20 and 24 of Tai. However, Fang et al. discloses a portion of an integrated circuit device comprising a shaped functional block, said functional block comprising a semiconductor material 2-3-4-7-8 with a light-emitting diode, specifically a gallium arsenide light-emitting diode. Note figure 2 of Fang et al. Therefore, it would have been obvious to a person having skill in the art to augment Tai's portion of an integrated circuit device comprising a shaped comprising a semiconductor material, with the light-emitting diode, specifically the gallium arsenide light-emitting diode such as taught by Fang et al. in order to provide a device having silicon active circuits for logic and power, along with high energy band gap II-V active circuits for optoelectronics, to thus merge semiconductor optoelectronics with silicon technology.

(3) Tai discloses an electronic chip comprising a block of material separated from a substrate and having a first surface and a second surface substantially parallel to said first surface, having all the limitations of claims 94-97 except that said electronic chip is a light-emitting diode or a gallium arsenide diode, specifically a gallium arsenide microwave device, more specifically a gallium arsenide resonant tunneling diode. Note figures 1,3,4, column 2 lines 45-49, and column 3 lines 20 and 24 of Tai. However, Fang et al. discloses a block of material 2-3-4-7-8 separated from a substrate 10 and having a first surface and a second surface substantially parallel to said first surface with a light-emitting diode or a gallium arsenide diode, specifically a gallium arsenide microwave device, more specifically a gallium arsenide resonant tunneling diode. Note figure 2 of Fang et al. Therefore, it would have been obvious to a person having skill in the art to augment Tai's electronic chip comprising a block of material separated from a substrate and having a first surface and a second surface substantially parallel to said first surface with the light-emitting diode or a gallium arsenide diode, specifically a gallium arsenide microwave device, more specifically a gallium arsenide resonant tunneling diode such as taught by Fang et al. in order to provide a device having silicon active circuits for logic and power, along with high energy band gap II-V active circuits for optoelectronics, to thus merge semiconductor optoelectronics with silicon technology.

(4) Tai discloses an electronic chip comprising a shaped functional block including a semiconductor material that is a multilayered structure, having all the limitations of claim 103 except that said multilayered structure constitutes a light-emitting diode. Note figures

1,3,4, column 2 lines 45-49, and column 3 lines 20 and 24 of Tai. However, Fang et al. discloses an electronic chip comprising a shaped functional block including a semiconductor material that is a multilayered structure 2-3-4-7-8 with a light-emitting diode. Note figure 2 of Fang et al. Therefore, it would have been obvious to a person having skill in the art to augment Tai's electronic chip comprising a shaped functional block including a semiconductor material that is a multilayered structure with the light-emitting diode such as taught by Fang et al. in order to provide a device having silicon active circuits for logic and power, along with high energy band gap II-V active circuits for optoelectronics, to thus merge semiconductor optoelectronics with silicon technology.

E. Claims 72-74,76-78,159, and 160 are rejected under 35 U.S.C. 103(a) as being unpatentable over TSUNETSUGU et al. (JP 05304306) in view of GARDNER et al. (5055892).

Tsunetsugu et al. discloses a semiconductor microstructure comprising a multilayered shaped block 11 including gallium arsenide, a group III-V compound, having a first (top) surface substantially parallel to a second (bottom) surface, said first surface having an associated first area, said second surface having an associated second area, said first area being larger than said second area, an edge 4 adjacent to said first surface being sloped. Note figures 8 and 13 of Tsunetsugu et al. Note that paragraph 0010 of Tsunetsugu et al. clearly states that the edge 4 is sloped at an angle of about 55 degrees. Tsunetsugu et al. does not disclose that said block has a maximum length dimension less than or equal to 1 mm in measure (about 500 microns or less in measure, per claim 159,

about 50 microns or less in measure, per claim 160). Tsunetsugu et al. does not disclose the 50 micron to 1 mm scale for said block as claimed by the applicant, in fact Tsunetsugu et al. makes no mention whatsoever of any kind of scale for said block. Given that Tsunetsugu et al.'s device is in fact fully disclosed, this lack of mention indicates that it may have been within the skill of one having skill in the art to determine the proper scale for himself.

Gardner et al. discloses a device with a multilayered shaped block, being in Gardner et al.'s version a functioning LED having typical dimensions of 250 microns length, breadth, and depth. Note column 6 lines 25-26 Gardner et al. Therefore, it would have been obvious to a person having skill in the art to scale Tsunetsugu et al.'s multilayered shaped block in the ranges 50 microns to 1 mm, such as taught by Gardner et al. in order to build the multilayered shaped block in the scale ranges typically known to the art at the time of the invention. Although neither Gardner et al. nor Tsunetsugu et al. disclose the 50 micron scale for the multilayered shaped block it has recently been observed that a *prima facie* case of obviousness typically exists when the ranges of a component of the claimed invention overlap the ranges disclosed in the prior art or when the ranges of the component do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. *In re Peterson*, 65 USPQ2d 1379 (CA FC 2003). It appears that in this case, one skilled in the art would have expected a 50 micron multilayered shaped block to have the same properties as the 250 micron multilayered shaped block disclosed by Gardner et al.

F. Claims 87,169, and 170 are rejected under 35 U.S.C. 103(a) as being unpatentable over NG et al. (H208) in view of GARDNER et al. (5055892).

Ng et al. discloses an electronic chip comprising a block of material having all the limitations of claims 169,170, and 87 except that said block of material has a width of about 1 mm or less (500 microns or less, per claim 170, 50 microns or less, per claim 87) and a length of about 1 mm or less (500 microns or less, per claim 170, 50 microns or less, per claim 87). Note the explanation regarding claim 86 in section 7B above. Ng et al. does not disclose the 50-micron to 1 mm scale for the block of material as claimed by the applicant.

Gardner et al. discloses a device with a block of material, being in Gardner et al.'s version a functioning LED, having typical dimensions of 250 microns length, breadth, and depth. Note column 6 lines 25-26 Gardner et al. Therefore, it would have been obvious to a person having skill in the art to scale Ng et al.'s block of material in the ranges 50 microns to 1 mm, such as taught by Gardner et al. in order to build the block of material in the scale ranges typically known to the art at the time of the invention. Although neither Gardner et al. nor Ng et al. disclose the 50 micron scale for the block of material it has recently been observed that a *prima facie* case of obviousness typically exists when the ranges of a component of the claimed invention overlap the ranges disclosed in the prior art or when the ranges of the component do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. *In re Peterson*, 65 USPQ2d 1379 (CA FC 2003). It appears that in this case, one skilled in the art

would have expected a 50 micron block of material to have the same properties as the 250 micron block of material disclosed by Gardner et al.

G. Claims 111-122 and 181-185 are rejected under 35 U.S.C. 103(a) as being unpatentable over FANG et al. (IBM Technical Disclosure, vol. 19, No. 10, Mar. 1977, pp. 3959-3960) in view of TAI (4670770).

Fang et al. discloses a light-emitting diode (LED) 2-3-4-7-8, incorporated in an active display 1, comprising a shaped multilayered gallium arsenide (a group III-V compound) semiconductor block 2-3-4 comprising a first surface and a second surface in substantially parallel relation to said first surface. Alternately, Fang et al. discloses a light-emitting diode (LED) comprising an amount of gallium arsenide (a group III-V compound) semiconductor material 2-3-4, said semiconductor material 2-3-4 having a first surface, the perimeter of said first surface having a rectangular shape, in substantially parallel relation to a second surface, Note figures 1 and 2 of Fang et al. Fang et al. does not disclose that said semiconductor block has a length dimension less than or equal to 1 mm in measure, less than or equal to 500 microns in measure, and in fact less than or equal to 50 microns, or that said semiconductor block has etched tapered sides, to define at least a beveled edge to a first surface, so that the tapered sides are non-parallel side surfaces connecting said first surface to a second surface so that said second surface is smaller than said first surface.

However, Tai discloses an array including shaped multilayered gallium arsenide semiconductor blocks 11-12-13-14-15-16, each semiconductor block having a length di-

mension less than or equal to 1 mm in measure, less than or equal to 500 microns in measure, and in fact less than or equal to 50 microns, and etched tapered sides to define at least a beveled edge to a first surface, so that the tapered sides are non-parallel side surfaces connecting said first surface to a second surface, and said second surface is smaller than said first surface. Note figure 1 of Tai. Therefore, it would have been obvious to a person having skill in the art to replace the shaped multilayered semiconductor blocks of Fang et al.'s light-emitting diode with the shaped multilayered gallium arsenide semiconductor blocks (11-12-13-14-15-16), each semiconductor block having a length dimension less than or equal to 1 mm in measure, less than or equal to 500 microns in measure, and in fact less than or equal to 50 microns, and etched tapered sides to define at least a beveled edge to a first surface, so that the tapered sides are non-parallel side surfaces connecting said first surface to a second surface, and said second surface is smaller than said first surface such as taught by Tai. One would be motivated to do so, because, as Tai points out, the shaped multilayered gallium arsenide semiconductor blocks align better to a silicon substrate when the edges are angled.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Mon-Thu 8-6.Any inquiry concerning this communication or earlier communications from the examiner should be directed to

Thomas L Dickey whose telephone number is 703-308-0980. The examiner can normally be reached on Tues-Friday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

TLD
08/2002

Minhloan Tran
Primary Examiner
Art Unit 2826